STRUCTURES AND METHODS OF TESTING INTERCONNECT STRUCTURES IN PROGRAMMABLE LOGIC DEVICES

ABSTRACT

Structures enabling the efficient testing of interconnect in programmable logic devices (PLDs), and methods utilizing these structures. A PLD includes a non-homogeneous array of programmable logic blocks and an array of standardized interconnect blocks, where the same interconnect block is used for different types of logic blocks. Coupled between each of the interconnect blocks and the associated logic block is a standardized test structure, allowing the same test configuration to be used for each interconnect block even though the interconnect blocks are associated with logic blocks of different types. In some embodiments, one or more types of logic blocks are not associated with standardized test structures. These logic blocks are coupled directly to their associated interconnect blocks, and are preferably of a type that can be configured to emulate the standardized test structure. Thus, by a correct application of configuration data all of the interconnect blocks display the same behavior.